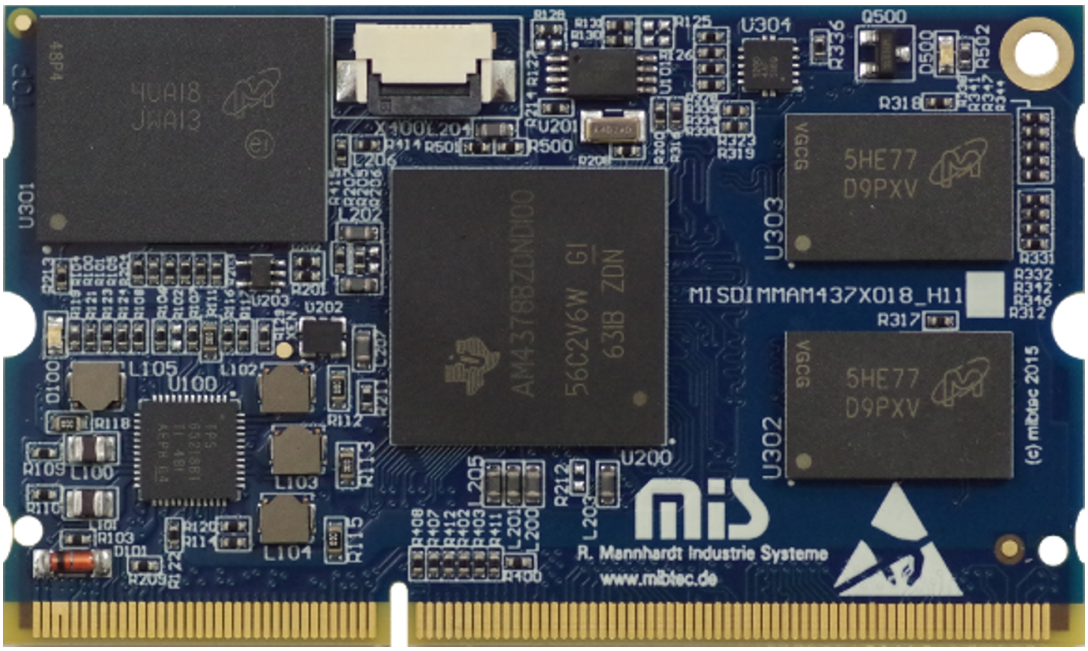
MIS R. Mannhardt Industrie Systeme

Datasheet

MIS-DIMM-AM437X System on Module

Texas Instruments Sitara AM437x based System-on-Module



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1 . About this Document

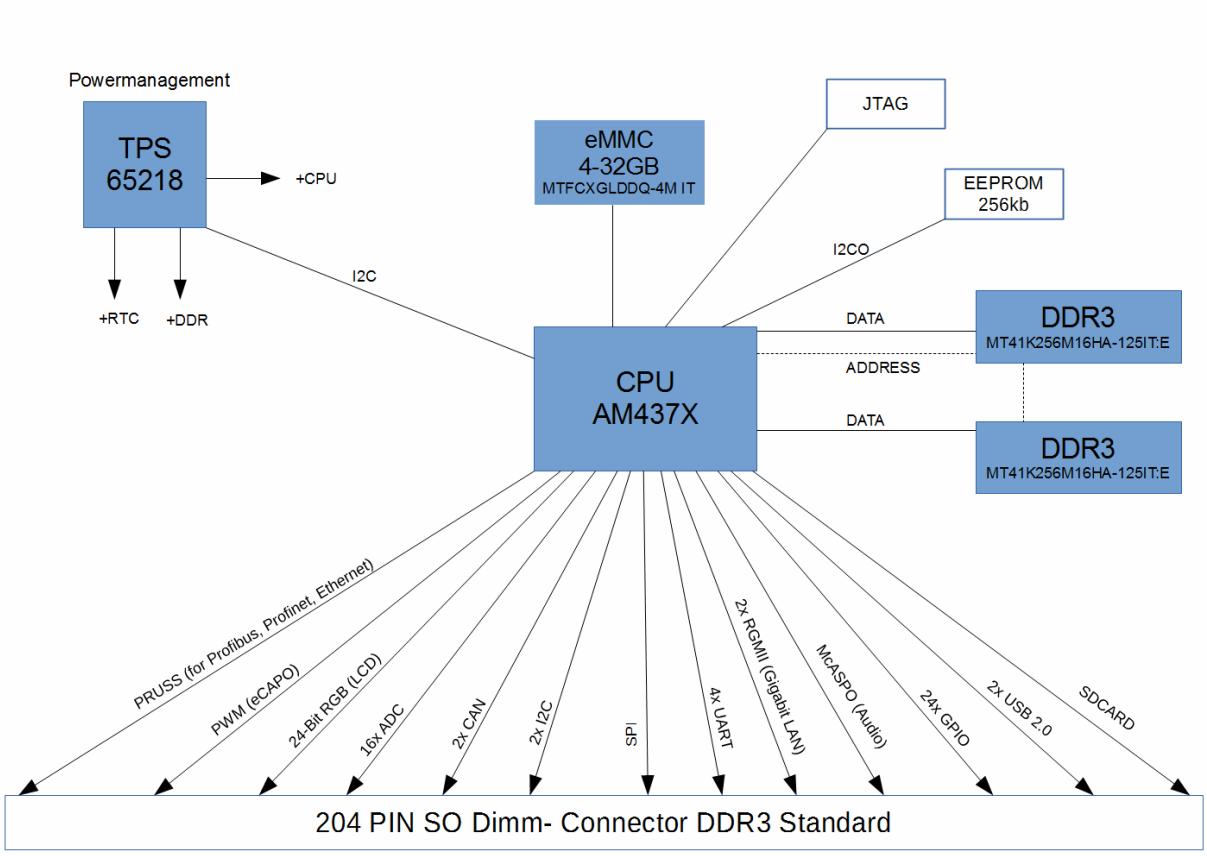
1.1 Overview

The MIS-DIMM-AM437X is a SODIMM-DDR3 standard with 204 Pins System-on-Module designed as a building block for integration into embedded applications. It is built around the Texas Instruments Sitara AM437x processor family featuring an advanced ARM Cortex-A9 ARM CPU coupled with a PowerVR SGX GPU. The MIS-DIMM-AM437X is supplemented with up-to 2GB DDR3L and 32GB of on-board eMMC storage. The MIS-DIMM-AM437X supports TFT Displays up to 2048 x 2048 bpp and resistive or capacitive touch panels. The possibility to work with different operating systems such as Openembedded/Yocto/Poky Linux and Android makes our SoM extreme flexible.

1.2 MIS-DIMM-AM437X Features Summary

- High Performance 1 GHz Cortex-A9 TI Processor
- Quad 200 MHz programmable real-time unit (PRU)
- PowerVR™ SGX530 graphics core
- up to 2048 MB DDR3L
- up to 32 GB eMMC
- supports TFT Displays up to 2048 x 2048 bpp 24 bit RGB
- Capacitive and resistive touch panel interfaces
- 2 x Gigabit Ethernet
- 3 x I2C
- McASP, JTAG, SPI
- Profibus, Profinet, Ethercat
- 4 x UART
- 16 ADC inputs
- 2 x USB 2.0 Host/OTG
- 3V – 5,5V
- 67.6 mm x 40 mm x 3.1 mm DDR3 SODIMM 204pins footprint

1.3 MIS-DIMM-AM437X Block Diagram



2 . Main Components

2.1 Texas Instruments Sitara™ AM437x ARM® Cortex™ -A9

Highlights

- Sitara™ARM® Cortex® -A9 32-Bit RISC Processor With Processing Speed Up to 1000-MHz ARM® Cortex™-A9 32-Bit RISC Microprocessor
  - NEON™ SIMD Coprocessor and Vector Floating Point (VFPv3) Coprocessor
  - 32KB of Both L1 Instruction and Data Cache
  - 256KB of L2 Cache or L3 RAM
- 32-Bit LPDDR2, DDR3, and DDR3L Support
- General-Purpose Memory Support (NAND, NOR, SRAM) Supporting Up to 16-bit ECC
- SGX530 Graphics Engine
- Display Subsystem
- Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)
- Real-Time Clock (RTC)
- Up to Two USB 2.0 High-Speed Dual-Role (Host or OTG) Ports with integrated PHY
- 10, 100, and 1000 Ethernet Switch Supporting Up to Two Ports
- Serial Interfaces:
  - Two Controller Area Network (CAN) Ports
  - Six UARTs, Two McASPs, Five McSPI, Three I2C Ports, One QSPI and One HDQ or 1-Wire
- Security
  - Crypto Hardware Accelerators (AES, SHA, RNG, DES and 3DES)
  - Secure Boot
- Two 12-Bit Successive Approximation Register (SAR) ADCs
- Up to Three 32-Bit Enhanced Capture Modules (eCAP)
- Up to Three Enhanced Quadrature Encoder Pulse Modules (eQEP)
- Up to Six Enhanced High-Resolution PWM Modules (eHRPWM)

MPU Subsystem

- Up to 1000-MHz ARM Cortex-A9 32-Bit RISC Microprocessor
- 32KB of Both L1 Instruction and Data Cache
- 256KB of L2 Cache (Option to Configure as L3 RAM)
- 256KB of On-Chip Boot ROM
- 64KB On-Chip RAM
- Secure Control Module (SCM)
- Emulation and Debug
  - JTAG
  - Embedded Trace Buffer
- Interrupt Controller

On-Chip Memory (Shared L3 RAM)

- 256KB of General Purpose On-Chip Memory Controller (OCMC) RAM
- Accessible to All Masters
- Supports Retention for Fast Wakeup
- Up to 512KB of Total Internal RAM (256KB of ARM Memory Configured as L3 RAM + 256KB of OCMC RAM)
-

External Memory Interfaces (EMIF)

- DDR Controllers:
  - LPDDR2: 266-MHz Clock (LPDDR2-533 Data Rate)
  - DDR3 and DDR3L: 400-MHz Clock (DDR 800 Data Rate)
  - 32-Bit Data Bus
  - 2GB of Total Addressable Space
  - Supports One x32, Two x16, or Four x8 Memory Device Configurations
  -

General-Purpose Memory Controller (GPMC)

- Flexible 8- and 16-Bit Asynchronous Memory Interface with Up to Seven Chip Selects (NAND, NOR, Muxed-NOR, and SRAM)

- Uses BCH Code to Support 4-, 8-, or 16-Bit ECC
- Uses Hamming Code to Support 1-Bit ECC
-

Error Locator Module (ELM)

- Used with the GPMC to Locate Addresses of Data Errors from Syndrome Polynomials Generated Using a BCH Algorithm
- Supports 4-, 8-, and 16-Bit Per 512-Byte Block Error Location Based on BCH Algorithms

Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)

- Supports Protocols such as EtherCAT®, PROFIBUS, PROFINET, and EtherNet/IP™, EnDat 2.2, and More
- Two Programmable Real-Time Units (PRUs) Subsystems
  - Each core is a 32-Bit Load and Store RISC Processor Capable of Running at 200 MHz
  - 12KB (PRU-ICSS1), 4KB (PRU-ICSS0) of Instruction RAM with Single-Error Detection (Parity)
  - 8KB (PRU-ICSS1), 4KB (PRU-ICSS0) of Data RAM with Single-Error Detection (Parity)
  - Single-Cycle 32-Bit Multiplier with 64-Bit Accumulator
  - Enhanced GPIO Module Provides Shift-In and Shift-Out Support and Parallel Latch on External Signal
- 12KB (PRU-ICSS1 only) of Shared RAM with Single-Error Detection (Parity)
- Three 120-Byte Register Banks Accessible by Each PRU
- Interrupt Controller Module (INTC) for Handling System Input Events
- Local Interconnect Bus for Connecting Internal and External Masters to the Resources Inside the PRU-ICSS
- Peripherals Inside the PRU-ICSS
  - One UART Port with Flow Control Pins, Supports Up to 12 Mbps
  - One Enhanced Capture (eCAP) Module
  - Two MII Ethernet Ports that Support Industrial Ethernet, such as EtherCAT
  - One MDIO Port
- Industrial Communication is Supported by Two PRU-ICSS Subsystems

Power Reset and Clock Management (PRCM) Module

- Controls the Entry and Exit of Deep-Sleep Modes
- Responsible for Sleep Sequencing, Power Domain Switch-Off Sequencing, Wake-Up Sequencing, and Power Domain Switch-On Sequencing
- Clocks
  - Integrated High-Frequency Oscillator Used to Generate a Reference Clock (19.2, 24, 25, and 26 MHz) for Various System and Peripheral Clocks
  - Supports Individual Clock Enable and Disable Control for Subsystems and Peripherals to Facilitate Reduced Power Consumption
  - Five ADPLLs to Generate System Clocks (MPU Subsystem, DDR Interface, USB, and Peripherals (MMC and SD, UART, SPI, I2C), L3, L4, Ethernet, GFX (SGX530), and LCD Pixel Clock)
- Power
  - Two Non-Switchable Power Domains (RTC and Wake-Up Logic (WAKE-UP))
  - Three Switchable Power Domains (MPU Subsystem, SGX530 (GFX), Peripherals and Infrastructure (PER))
  - Dynamic Voltage Frequency Scaling (DVFS)

Real-Time Clock (RTC)

- Real-Time Date (Day, Month, Year, and Day of Week) and Time (Hours, Minutes, and Seconds) Information
- Internal 32.768-kHz Oscillator, RTC Logic, and 1.1-V Internal LDO
- Independent Power-On-Reset (RTC_PWRONRSTn) Input
- Dedicated Input Pin (RTC_WAKEUP) for External Wake Events
- Programmable Alarm Can Generate Internal Interrupts to the PRCM for Wake Up or Cortex-A9 for Event Notification
- Programmable Alarm Can Be Used with External Output (RTC_PMIC_EN) to Enable the Power Management IC to Restore Non-RTC Power Domains

Peripherals

- Up to Two USB 2.0 High-Speed OTG Ports with Integrated PHY

- Up to Two Industrial Gigabit Ethernet MACs (10, 100, and 1000 Mbps)
  - Integrated Switch
  - Each MAC Supports MII, RMII, and RGMII and MDIO Interfaces
  - Ethernet MACs and Switch Can Operate Independent of Other Functions
  - IEEE 1588v2 Precision Time Protocol (PTP)
- Up to Two Controller-Area Network (CAN) Ports
  - Supports CAN Version 2 Parts A and B
- Up to Two Multichannel Audio Serial Ports (McASP)
  - Transmit and Receive Clocks Up to 50 MHz
  - Up to Four Serial Data Pins Per McASP Port with Independent TX and RX Clocks
  - Supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and Similar Formats
  - Supports Digital Audio Interface Transmission (SPDIF, IEC60958-1, and AES-3 Formats)
  - FIFO Buffers for Transmit and Receive (256 Bytes)
- Up to Six UARTs
  - All UARTs Support IrDA and CIR Modes
  - All UARTs Support RTS and CTS Flow Control
  - UART1 Supports Full Modem Control
- Up to Five Master and Slave McSPI Serial Interfaces
  - McSPI0-McSPI2 Supports Up to Four Chip Selects
  - McSPI3-McSPI4 Supports Up to Two Chip Selects
  - Up to 48 MHz
- One Quad-SPI
  - Supports eXecute In Place (XIP) from Serial NOR FLASH
- One Dallas 1-Wire® and HDQ Serial Interface
- Up to Three MMC, SD, and SDIO Ports
  - 1-, 4-, and 8-Bit MMC, SD, and SDIO Modes
  - 1.8- or 3.3-V Operation on All Ports
  - Up to 48-MHz Clock
  - Supports Card Detect and Write Protect
  - Complies with MMC4.3 and SD and SDIO 2.0 Specifications
- Up to Three I2C Master and Slave Interfaces
  - Standard Mode (Up to 100 kHz)
  - Fast Mode (Up to 400 kHz)
- Up to Six Banks of General-Purpose I/O (GPIO)
  - 32 GPIOs per Bank (Multiplexed with Other Functional Pins)
  - GPIOs Can be Used as Interrupt Inputs (Up to Two Interrupt Inputs per Bank)
- Up to Three External DMA Event Inputs That Can Also be Used as Interrupt Inputs
- Twelve 32-Bit General-Purpose Timers
  - DMTIMER1 is a 1-ms Timer Used for Operating System (OS) Ticks
  - DMTIMER4–DMTIMER7 are Pinned Out
- One Public Watchdog Timer
- One Free Running High Resolution 32-kHz Counter (synctimer32K)
- SGX530 3D Graphics Engine
  - Tile-Based Architecture Delivering Up to 20M Poly/sec
  - Universal Scalable Shader Engine is a Multi- Threaded Engine Incorporating Pixel and Vertex Shader Functionality
  - Advanced Shader Feature Set in Excess of Microsoft VS3.0, PS3.0, and OGL2.0
  - Industry Standard API Support of Direct3D Mobile, OGL-ES 1.1 and 2.0, and OpenVG 1.0
  - Fine-Grained Task Switching, Load Balancing, and Power Management
  - Advanced Geometry DMA-Driven Operation for Minimum CPU Interaction
  - Programmable High-Quality Image Anti- Aliasing
  - Fully Virtualized Memory Addressing for OS Operation in a Unified Memory Architecture

Display Subsystem

- Display Modes
  - Programmable Pixel Memory Formats (Palletized: 1-, 2-, 4-, and 8-Bit Per Pixel; RGB 16- and 24-Bit Per Pixel; and YUV 4:2:2)
- 256 x 24-Bit Entries Palette in RGB
- Up to 2048 x 2048 Resolution

Display Support

- Four Types of Displays Are Supported: Passive and Active Colors; Passive and Active Monochromes

- 4- and 8-Bit Monochrome Passive Panel Interface Support (15 Grayscale Levels Supported Using Dithering Block)
- RGB 8-Bit Color Passive Panel Interface Support (3,375 Colors Supported for Color Panel Using Dithering Block)
- RGB 12-, 16-, 18-, and 24-Bit Active Panel Interface Support (Replicated or Dithered Encoded Pixel Values)
- Remote Frame Buffer (Embedded in the LCD Panel) Support through the RFBI Module
- Partial Refresh of the Remote Frame Buffer through the RFBI Module
- Partial Display
- Multiple Cycles Output Format on 8-, 9-, 12-, and 16-Bit Interface (TDM)

Signal Processing

- Overlay and Windowing Support for One Graphics Layer (RGB or CLUT) and Two Video Layers (YUV4:2:2, RGB16, and RGB24)
- RGB 24-bit Support on the Display Interface, Optionally Dithered to RGB 18-Bit Pixel Output Plus 6-Bit Frame Rate Control (Spatial and Temporal)
- Transparency Color Key (Source and Destination)
- Synchronized Buffer Update
- Gamma Curve Support
- Multiple-Buffer Support
- Cropping Support
- Color Phase Rotation
- Two 12-Bit Successive Approximation Register (SAR) ADCs (ADC0, ADC1)
  - 867K Samples Per Second
  - Input Can Be Selected from Any of the Eight Analog Inputs Multiplexed Through an 8:1 Analog Switch
  - ADC0 Can Be Configured to Operate as a 4-, 5-, or 8-Wire Resistive Touch Screen Controller (TSC)
- Up to Three 32-Bit Enhanced Capture Modules (eCAP)
  - Configurable as Three Capture Inputs or Three Auxiliary PWM Outputs
- Up to Six Enhanced High-Resolution PWM Modules (eHRPWM)
  - Dedicated 16-Bit Time-Base Counter with Time and Frequency Controls
  - Configurable as Six Single-Ended, Six Dual- Edge Symmetric, or Three Dual-Edge Asymmetric Outputs
- Up to Three 32-Bit Enhanced Quadrature Encoder Pulse (eQEP) Modules

Device Identification

- Factory Programmable Electrical Fuse Farm (FuseFarm)
  - Production ID
  - Device Part Number (Unique JTAG ID)
  - Device Revision (Readable by Host ARM)
  - Feature Identification

Debug Interface Support

- JTAG and cJTAG for ARM (Cortex-A9 and PRCM) and PRU-ICSS Debug
- Supports Real-Time Trace Pins (for Cortex-A9)
- 64KB Embedded Trace Buffer (ETB)
- Supports Device Boundary Scan
- Supports IEEE 1500

DMA

- On-Chip Enhanced DMA Controller (EDMA) Has Three Third-Party Transfer Controllers (TPTC) and One Third-Party Channel Controller (TPCC), Which Supports Up to 64 Programmable Logical Channels and Eight QDMA Channels
- EDMA is Used for:
  - Transfers to and from On-Chip Memories
  - Transfers to and from External Storage (EMIF, General-Purpose Memory Controller, and Slave Peripherals)

Inter-Processor Communication (IPC)

- Integrates Hardware-Based Mailbox for IPC and Spinlock for Process Synchronization Between the Cortex-A9, PRCM, and PRU-ICSS

Boot Modes

- Boot Mode is Selected via Boot Configuration Pins Latched on the Rising Edge of the PWRONRSTn Reset Input Pin

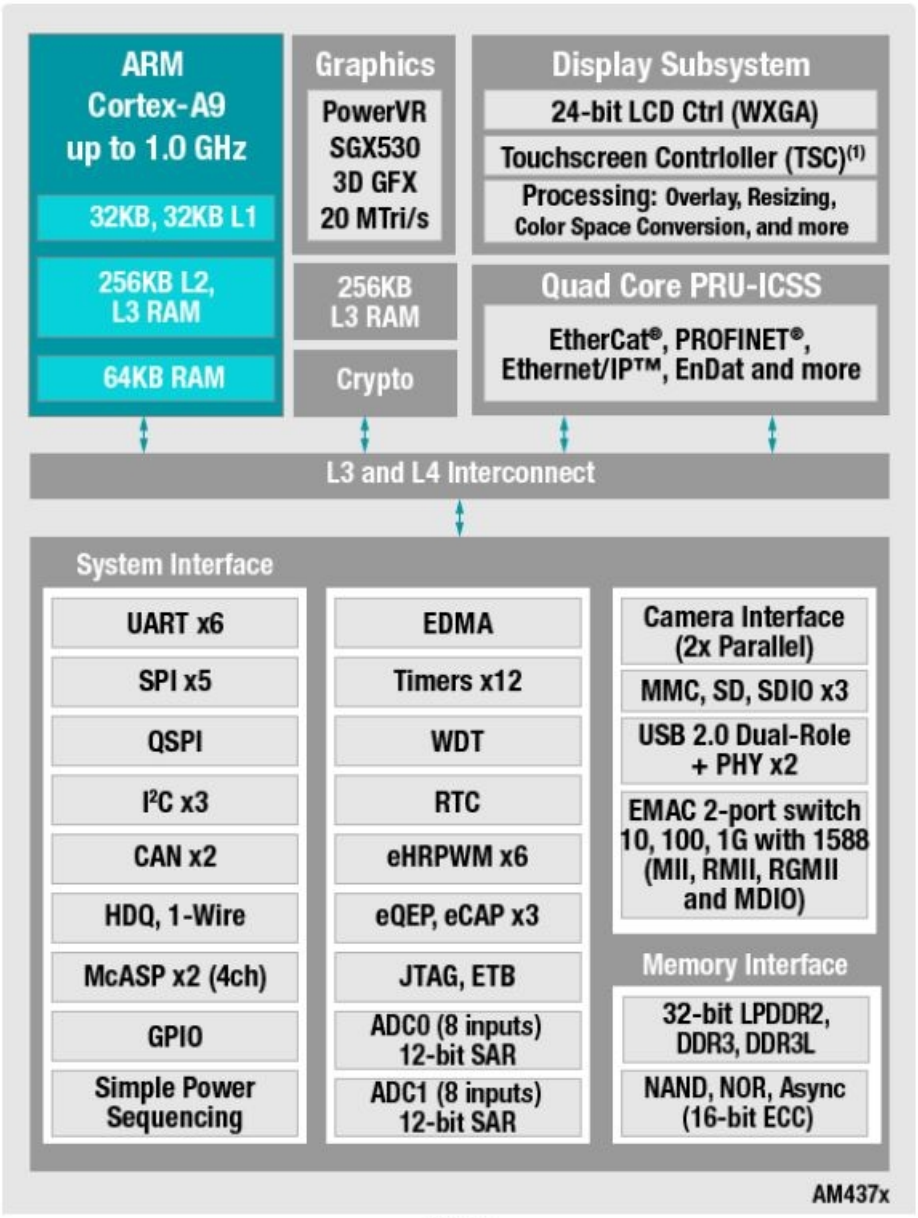
Camera

- Dual Port 8- and 10-Bit BT656 Interface
- Dual Port 8- and 10-Bit Including External Syncs
- Single Port 12-Bit
- YUV422/RGB422 and BT656 Input Format
- RAW Format
- Pixel Clock Rate Up to 75 MHz

Package

- 491-pin BGA Package (17x17 mm) (ZDN Suffix), 0.65-mm Ball Pitch with Via Channel Array Technology to Enable Low-Cost Routing

2.1.1 Functional Block Diagram



NOTES:
(1) Use of TSC will limit availability of channels on one ADC

2.2 TPS65218 Powermanagement

The Texas Instrument's TPS65218 is an integrated power-management IC dedicated to applications processors as the AM437x. The device provides:

BATTERY BACKUP SUPPLIES
- Two low-quiescent current, high efficiency step-down converters for battery backup domain
  - DCDC5: 1.0V output
  - DCDC6: 1.8V output
- VIN range from 2.2V to 5.5V
- Can be 7supplied from system power or coin-cell backup battery

BUCK CONVERTERS (DCDC1, 2, 3)
- Three adjustable step-down converter with integrated switching FETs
  - DCDC1: 1.1V default up to 1.8A (Core)
  - DCDC2: 1.1V default up to 1.8A (MPU)
  - DCDC3: 1.2V default up to 1.8A (DDR)
- VIN range from 2.7V to 5.5V
- Adjustable output voltage range 0.85V-3.5V
- 100% Duty Cycle for Lowest Dropout

LOW VOLTAGE LOAD SWITCH (LS1)
- VIN range from 1.2V to 3.3V
- 350mA current limit
- 110mA (max) switch impedance at 1.35V

HIGH-VOLTAGE LOAD SWITCH (LS3)
- VIN range from 1.8V to 10.0V
- 100mA / 500mA selectable current limit
- 500mA (max) switch impedance

SUPERVISOR
- Built-in supervisor function monitors
  - DCDC1, DCDC2, DCDC3 to +/-4%
  - DCDC4 and LDO1 to +/-5%

PROTECTION / DIAGNOSTICS / CONTROL
- Under voltage lockout
- Over temperature warning / shutdown
- Always-on push-button monitor
- Separate power-good output for backup
- Open-drain interrupt output pin
- User programmable default voltages and power sequencing
- I2C interface (Address 0x24h)

TPS65218 features are utilized internally by the MIS-DIMM-AM437X and are not exposed to the 204 pin connector.

2.3 Memory

2.3.1 RAM MT41K256M16HA-125IT:E

The MIS-DIMM-AM437X is supplemented with up-to 2GB DDR3L memory.

DDR3L SDRAM (1.35V) is a low voltage version of the DDR3 (1.5V) SDRAM. Refer to the DDR3 (1.5V) SDRAM data sheet specifications when running in 1.5V compatible mode.

2.3.2 eMMC MTFCXGLDDQ-4M IT

The MIS-DIMM-AM437X is available with up to 32GB of storage.

2.4 Ethernet

The MIS-DIMM-AM437X uses the two Industrial Gigabit Ethernet MACs (10, 100, and 1000 Mbps) interfaces of the Texas Instruments Sitara™ AM437x ARM® Cortex™ -A9 CPU.

2.5 Audio

The MIS-DIMM-AM437X uses the Multichannel Audio Serial Port (McASP) of the Texas Instruments Sitara™ AM437x ARM® Cortex™ -A9 CPU.

3 . External Connectors (204 Pin SODIMM)

PIN	BALL	Schematic Net Name	Powered
1	-	+PWR	+3V3
2	-	+PWR	+3V3
3	-	+PWR	+3V3
4	-	+PWR	+3V3
5	-	DGND	+3V3
6	-	DGND	+3V3
7	-	DGND	+3V3
8	-	DGND	+3V3
9	-	+3V3	+3V3
10	-	+3V3	+3V3
11	-	+3V3	+3V3
12	-	+3V3	+3V3
13	-	+1V8	+3V3
14	-	+1V8	+3V3
15	TSP44	TPS-PB	+3V3
16	TSP25	TPS-CC	+3V3
17	G22	SYS_RESETn	+3V3
18	TSP8 / Y23	PORZn	+3V3
19	TSP45 / G25	NMIn	+3V3
20	TSP19 / AE6	RTC_PORZn	+3V3
21	-	AGND	+3V3
22	-	AGND	+3V3
23	-	+ADC0_VREFP	+1V8
24	-	ADC1 AIN0	+1V8
25	AA12	ADC0 AIN0	+1V8
26	AC16	ADC1 AIN0	+1V8
27	Y12	ADC0 AIN1	+1V8
28	AB16	ADC1 AIN1	+1V8
29	Y13	ADC0 AIN2	+1V8
30	AA16	ADC1 AIN2	+1V8
31	AA13	ADC0 AIN3	+1V8
32	AB15	ADC1 AIN3	+1V8
33	AB13	ADC0 AIN4	+1V8
34	AA15	ADC1 AIN4	+1V8
35	AC13	ADC0 AIN5	+1V8
36	Y15	ADC1 AIN5	+1V8
37	AD13	ADC0 AIN6	+1V8
38	AE16	ADC1 AIN6	+1V8
39	AE13	ADC0 AIN7	+1V8

PIN	BALL	Schematic Net Name	Powered
40	AD16	ADC1 AIN7	+1V8
41	-	DGND	+3V3
42	-	DGND	+3V3
43	AE23	UART2 RXD	+3V3
44	AC21	UART1 RXD	+3V3
45	AD22	UART2 TXD	+3V3
46	AB20	UART1 TXD	+3V3
47	AE24	UART2 RTSn	+3V3
48	AE22	UART1 RTSn	+3V3
49	AD23	UART2 CTSn	+3V3
50	AD21	UART1 CTSn	+3V3
51	-	DGND	+3V3
52	-	DGND	+3V3
53	H24	UART3 TXD	+3V3
54	J24	UART0 TXD	+3V3
55	H25	UART3 RXD	+3V3
56	K25	UART0 RXD	+3V3
57	K24	UART3 RTSn	+3V3
58	J25	UART0 RTSn	+3V3
59	H22	UART3 CTSn	+3V3
60	L25	UART0 CTSn	+3V3
61	-	DGND	+3V3
62	-	DGND	+3V3
63	K22	CAN0 TX	+3V3
64	Y22	I2C0 SCL	+3V3
65	L22	CAN0 RX	+3V3
66	AB24	I2C0 SDA	+3V3
67	K21	CAN1 TX	+3V3
68	T20	I2C1 SCL	+3V3
69	L21	CAN1 RX	+3V3
70	T21	I2C1 SDA	+3V3
71	-	DGND	+3V3
72	-	DGND	+3V3
73	A24	DSS ACBIAS EN/SB18	+3V3
74	B23	DSS VSYNC/SB16	+3V3
75	A23	DSS HSYNC/SB17	+3V3
76	A22	DSS PCLK	+3V3
77	B22	DSS DATA0	+3V3
78	A21	DSS DATA1	+3V3
79	B21	DSS DATA2	+3V3
80	C21	DSS DATA3	+3V3

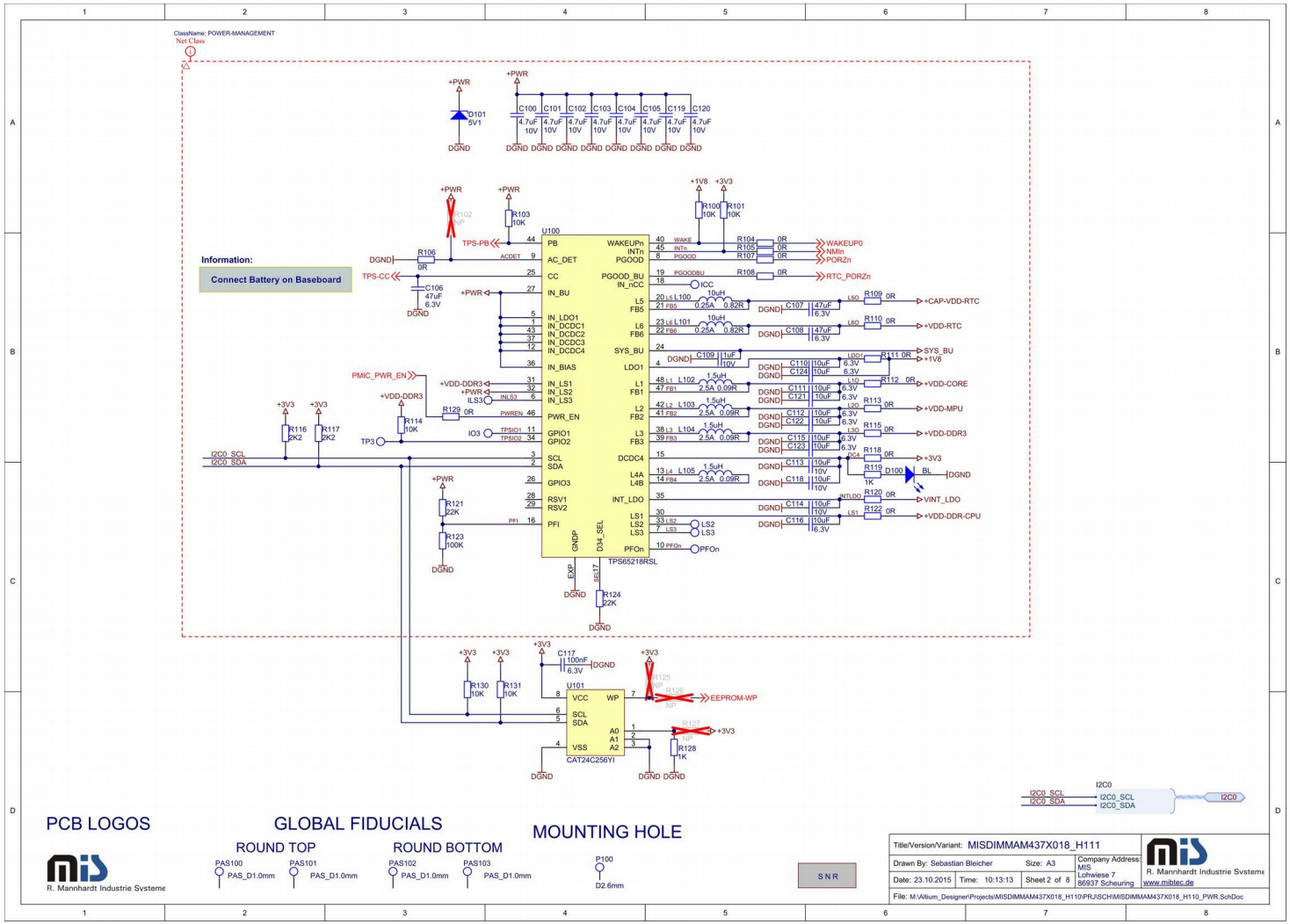
PIN	BALL	Schematic Net Name	Powered
81	A20	DSS DATA4	+3V3
82	B20	DSS DATA5/SB5	+3V3
83	C20	DSS DATA6/SB6	+3V3
84	E19	DSS DATA7/SB7	+3V3
85	A19	DSS DATA8/SB8	+3V3
86	B19	DSS DATA9/SB9	+3V3
87	A18	DSS DATA10/SB10	+3V3
88	B118	DSS DATA11/SB11	+3V3
89	C19	DSS DATA12/SB12	+3V3
90	D19	DSS DATA13/SB13	+3V3
91	C17	DSS DATA14/SB14	+3V3
92	D17	DSS DATA15/SB15	+3V3
93	AC24	DSS DATA16	+3V3
94	AA19	DSS DATA17	+3V3
95	AB19	DSS DATA18	+3V3
96	AC20	DSS DATA19	+3V3
97	AD17	DSS DATA20	+3V3
98	AC18	DSS DATA21	+3V3
99	AD18	DSS DATA22	+3V3
100	AE17	DSS DATA23	+3V3
101	-	DGND	+3V3
102	-	DGND	+3V3
103	A17	MDIO DATA0	+3V3
104	G24	DSSPWM0	+3V3
105	B17	MDIO CLK	+3V3
106	N24	SPI 1 SCLK	+3V3
107	D13	RGMII 1 RCLK	+3V3
108	N22	SPI 1 D0	+3V3
109	A15	RGMII 1 RCTL	+3V3
110	H23	SPI 1 D1	+3V3
111	F17	RGMII 1 RD0	+3V3
112	M24	SPI 1 CS0	+3V3
113	B16	RGMII 1 RD1	+3V3
114	AC23	SPI 1 CS2	+3V3
115	E16	RGMII 1 RD2	+3V3
116	AE21	SPI 1 CS3	+3V3
117	C14	RGMII 1 RD3	+3V3
118	-		+3V3
119	A13	RGMII 1 TCTL	+3V3
120	A16	MCASP1 AXR3	+3V3
121	D14	RGMII 1 TCLK	+3V3

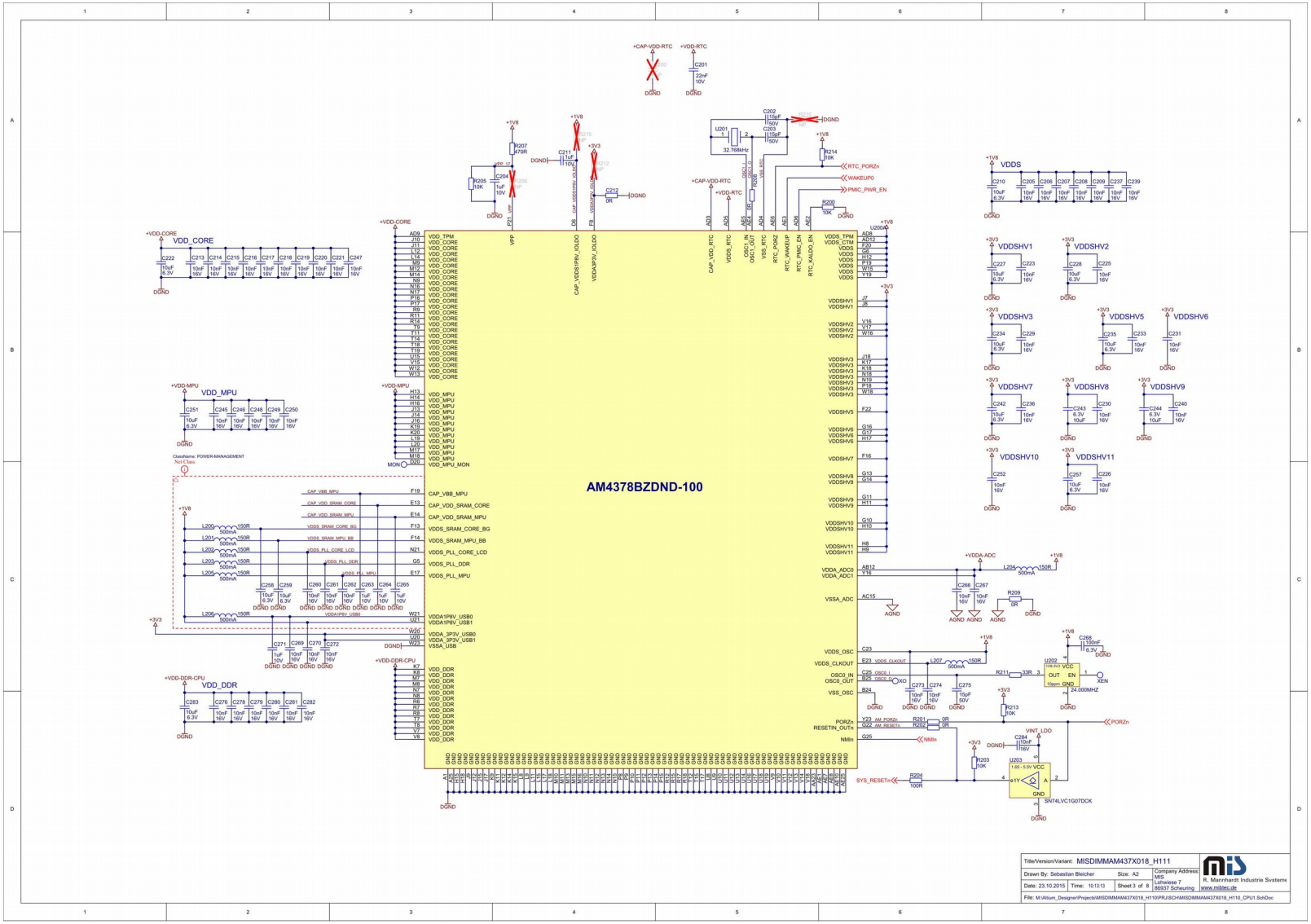
PIN	BALL	Schematic Net Name	Powered
122	D16	MCASP1 AXR2	+3V3
123	C16	RGMII 1 TD3	+3V3
124	D24	MCASP1 CLKOUT	+3V3
125	C13	RGMII 1 TD2	+3V3
126	B14	MCASP1 ACLKX	+3V3
127	A14	RGMII 1 TD1	+3V3
128	B13	MCASP1 FSX	+3V3
129	B15	RGMII 1 TD0	+3V3
130	-		+3V3
131	-	DGND	+3V3
132	-	DGND	+3V3
133	-		+3V3
134	-		+3V3
135	-	DGND	+3V3
136	-	DGND	+3V3
137	A17	MDIO DATA0	+3V3
138	C24	GPIO5 29	+3V3
139	B17	MDIO CLK	+3V3
140	D25	GPIO5 8	+3V3
141	F6	RGMII2 CLK	+3V3
142	F24	GPIO5 9	+3V3
143	C5	RGMII2 RCLK	+3V3
144	A9	GPIO2 2	+3V3
145	D8	RGMII2 RD0	+3V3
146	A8	GPIO1 29	+3V3
147	G8	RGMII2 RD1	+3V3
148	AE19	GPIO4 26	+3V3
149	B4	RGMII2 RD2	+3V3
150	B3	GPIO0 31	+3V3
151	F7	RGMII2 RD3	+3V3
152	A3	GPIO1 28	+3V3
153	C3	RGMII2 TCTL	+3V3
154	T22	GPIO0 3	+3V3
155	E8	RGMII2 TCLK	+3V3
156	C10	GPIO2 5	+3V3
157	C6	RGMII2 TD3	+3V3
158	P22	GPIO0 20	+3V3
159	A4	RGMII2 TD2	+3V3
160	P23	GPIO0 2	+3V3
161	D7	RGMII2 TD1	+3V3
162	L24	GPIO3 21	+3V3

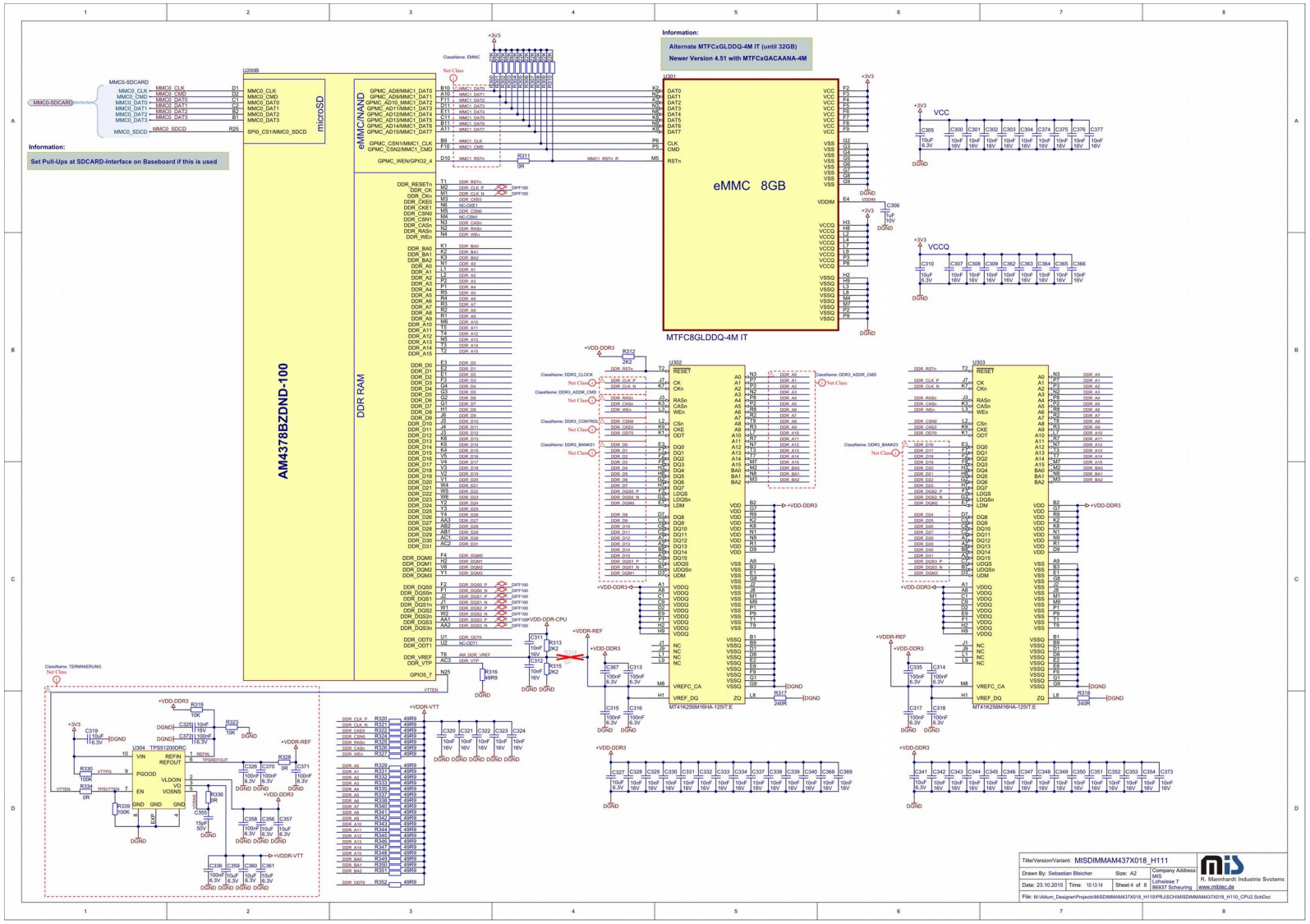
PIN	BALL	Schematic Net Name	Powered
163	E7	RGMII2 TD0	+3V3
164	P24	GPIO5 6	+3V3
165	-		+3V3
166	H20	GPIO0 24	+3V3
167	-	DGND	+3V3
168	-	DGND	+3V3
169	-		+3V3
170	G20	GPIO5 10	+3V3
171	-		+3V3
172	P25	GPIO5 4	+3V3
173	W24	USB0 D N	+3V3
174	AE20	GPIO4 28	+3V3
175	W25	USB0 D P	+3V3
176	K23	GPIO0 19	+3V3
177	W22	USB0 CE	+3V3
178	A2	GPIO0 30	+3V3
179	U24	USB0 ID	+3V3
180	L23	GPIO0 18	+3V3
181	U23	USB0 VBUS	+3V3
182	AB25	GPIO4 13	+3V3
183	G21	USB0 DRVVBUS	+3V3
184	AC25	GPIO4 12	+3V3
185	-		+3V3
186	AD20	GPIO4 29	+3V3
187	-	DGND	+3V3
188	-	DGND	+3V3
189	-		+3V3
190	D1	MMC0 CLK	+3V3
191	V24	USB1 D N	+3V3
192	D2	MMC0 CMD	+3V3
193	V25	USB1 D P	+3V3
194	C1	MMC0 DAT0	+3V3
195	U22	USB1 CE	+3V3
196	C”	MMC0 DAT1	+3V3
197	U25	USB1 ID	+3V3
198	B2	MMC0 DAT2	+3V3
199	T25	USB1 VBUS	+3V3
200	B1	MMC0 DAT3	+3V3
201	F25	USB1 DRVVBUS	+3V3
202	R25	MMC0 SDCD	+3V3
203	-	DGND	+3V3

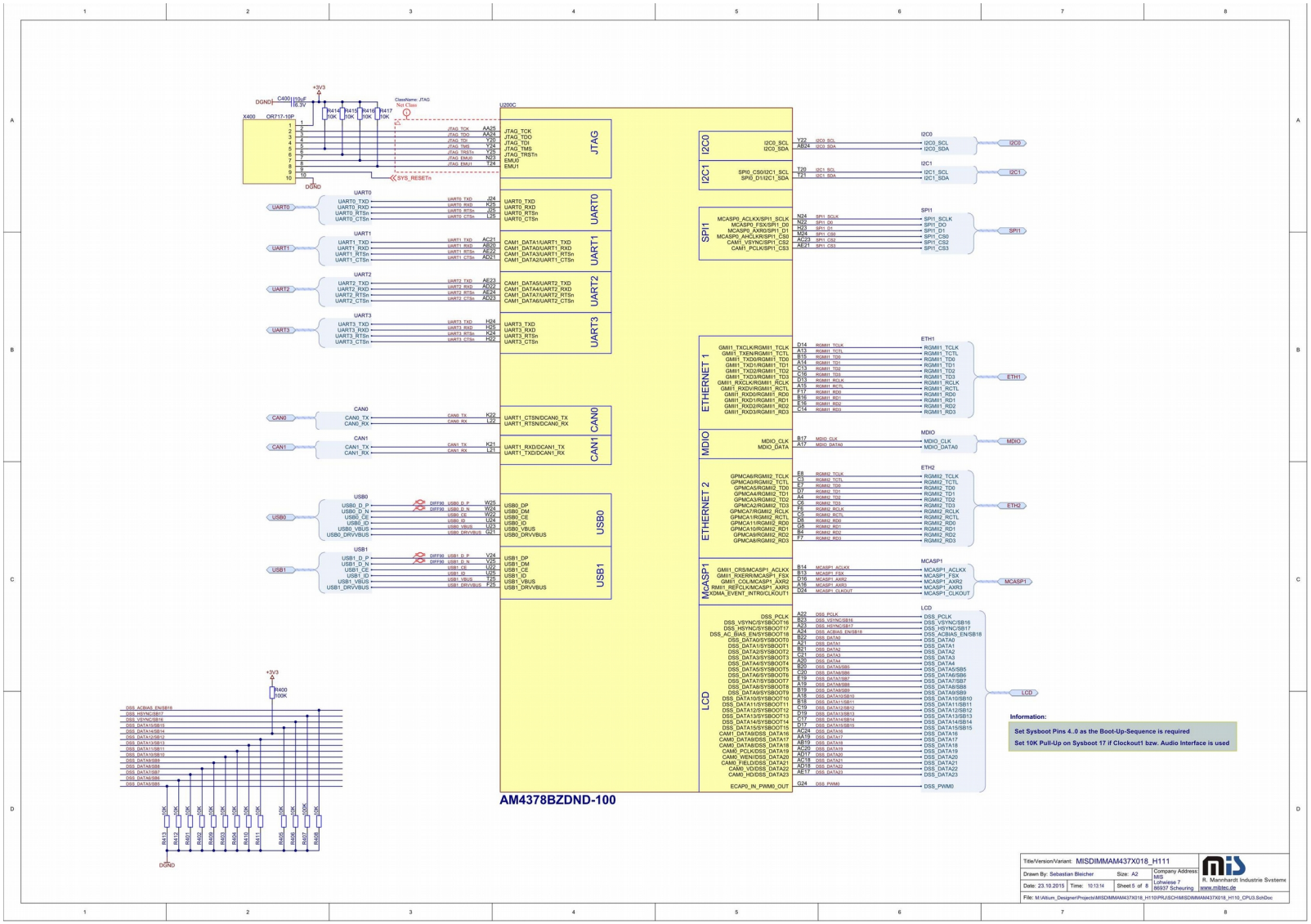
PIN	BALL	Schematic Net Name	Powered
204	-	DGND	+3V3

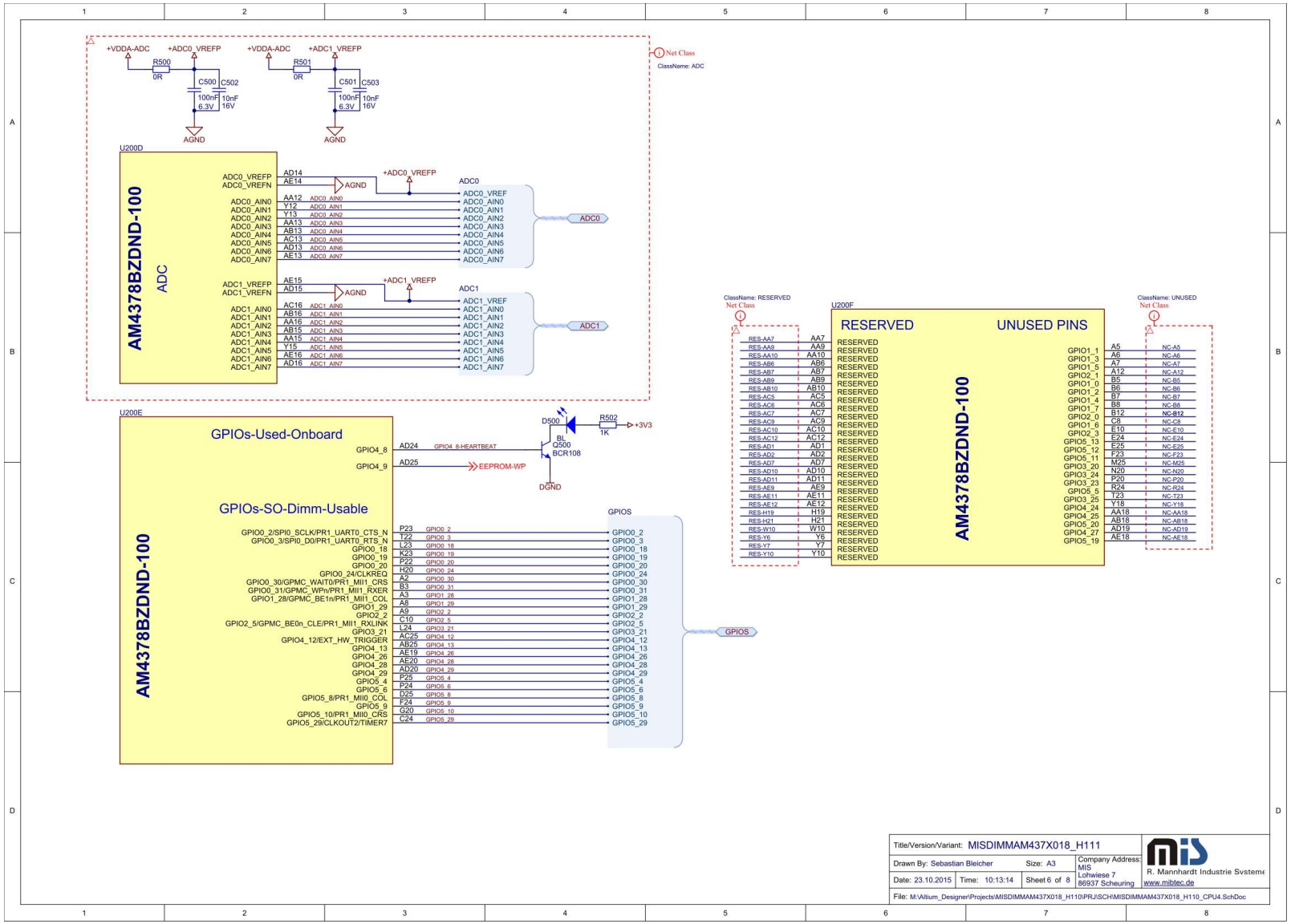
4 . Circuit diagram

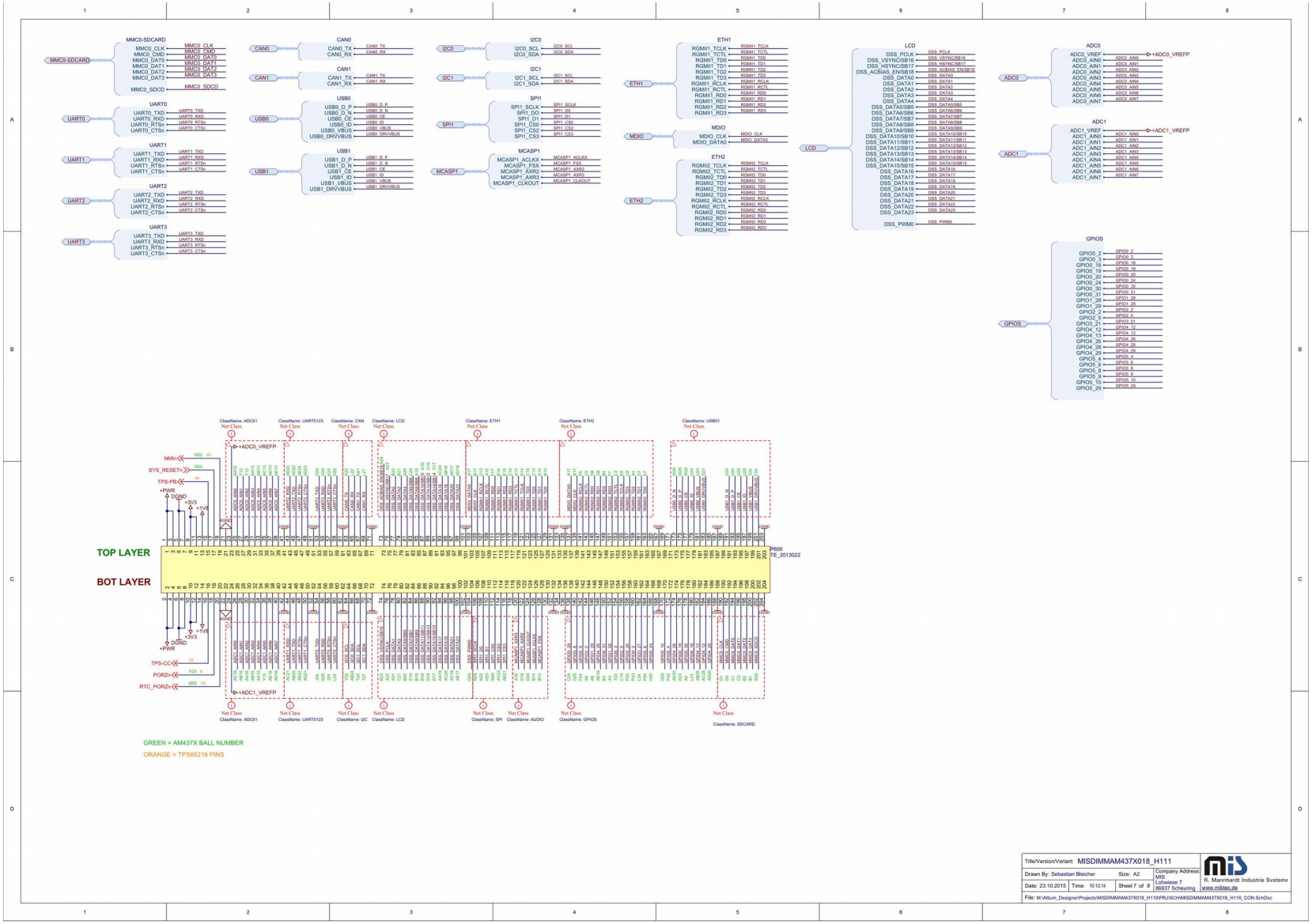



AM4378BZDND-100
VDD_CORE
VDD_MPU
VDD_DDR
VDDS
VDDSHV1
VDDSHV2
VDDSHV3
VDDSHV5
VDDSHV6
VDDSHV7
VDDSHV8
VDDSHV9
VDDSHV10
VDDSHV11
MISDIMMAM437X018_H111
R. Mannhardt Industrie Systeme
www.mbtec.de

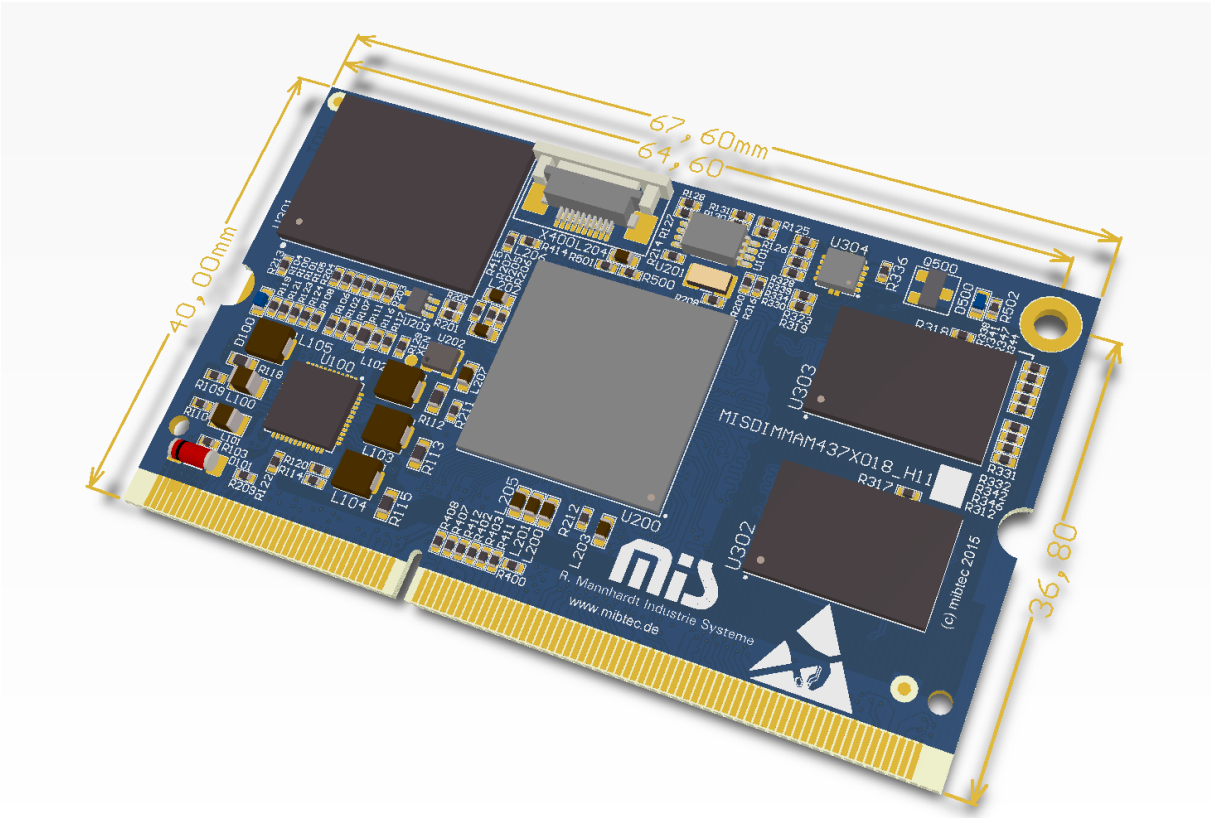

Information:
Alternate MTFCxGLDDQ-4M IT (until 32GB)
Newer Version 4.51 with MTFCxGACAANA-4M
Information:
Set Pull-Ups at SDCARD-Interface on Baseboard if this is used
AM4378BZDND-100
DDR RAM
eMMC/NAND
microSD
eMMC 8GB
MTFC8GLDDQ-4M IT
MT41K256M16HA-125IT:E
MISDIMMAM437X018_H111
R. Mannhardt Industrie Systems
23.10.2015
Sheet 4 of 8


AM4378BZDND-100
JTAG
UART0
UART1
UART2
UART3
CAN0
CAN1
USB0
USB1
I2C0
I2C1
SPI1
MDIO
ETHERNET 1
ETHERNET 2
McASP1
LCD
Information:
Set Sysboot Pins 4..0 as the Boot-Up-Sequence is required
Set 10K Pull-Up on Sysboot 17 if Clockout1 bzw. Audio Interface is used
Title/Version/Variant: MISDIMMAM437X018_H111
Company Address: MIS Lohmeise 7 66937 Schwing
R. Mannhardt Industrie Systeme
www.mbtec.de


+VDDA-ADC
+ADC0_VREFP
R500
0R
C500
100nF
6.3V
C502
10nF
16V
AGND
+ADC1_VREFP
R501
C501
C503
Net Class
ClassName: ADC
U200D
AM4378BZDND-100
ADC
ADC0_VREFP
ADC0_VREFN
ADC0_AIN0
ADC0_AIN1
ADC0_AIN2
ADC0_AIN3
ADC0_AIN4
ADC0_AIN5
ADC0_AIN6
ADC0_AIN7
ADC0
ADC1_VREFP
ADC1_VREFN
ADC1_AIN0
ADC1_AIN1
ADC1_AIN2
ADC1_AIN3
ADC1_AIN4
ADC1_AIN5
ADC1_AIN6
ADC1_AIN7
ADC1
U200E
GPIOs-Used-Onboard
GPIO4_8
GPIO4_9
AD24
GPIO4_8-HEARTBEAT
AD25
EEPROM-WP
D500
BL
Q500
BCR108
R502
1K
+3V3
DGND
GPIOs-SO-Dimm-Usable
GPIO0_2/SPI0_SCLK/PR1_UART0_CTS_N
GPIO0_3/SPI0_D0/PR1_UART0_RTS_N
GPIO0_18
GPIO0_19
GPIO0_20
GPIO0_24/CLKREQ
GPIO0_30/GPMC_WAIT0/PR1_MII1_CRS
GPIO0_31/GPMC_WPn/PR1_MII1_RXER
GPIO1_28/GPMC_BE1n/PR1_MII1_COL
GPIO1_29
GPIO2_2
GPIO2_5/GPMC_BE0n_CLE/PR1_MII1_RXLINK
GPIO3_21
GPIO4_12/EXT_HW_TRIGGER
GPIO4_13
GPIO4_26
GPIO4_28
GPIO4_29
GPIO5_4
GPIO5_6
GPIO5_8/PR1_MII0_COL
GPIO5_9
GPIO5_10/PR1_MII0_CRS
GPIO5_29/CLKOUT2/TIMER7
GPIOS
ClassName: RESERVED
Net Class
U200F
RESERVED
UNUSED PINS
AM4378BZDND-100
ClassName: UNUSED
Net Class
Title/Version/Variant: MISDIMMAM437X018_H111
Drawn By: Sebastian Bleicher
Size: A3
Date: 23.10.2015
Time: 10:13:14
Sheet 6 of 8
Company Address:
MIS
Lohwiese 7
86937 Scheuring
R. Mannhardt Industrie Systeme
www.mibtec.de
File: M:\Altium_Designer\Projects\MISDIMMAM437X018_H110\PRJSCH\MISDIMMAM437X018_H110_CPU4.SchDoc


MMC0-SDCARD
UART0
UART1
UART2
UART3
CAN0
CAN1
USB0
USB1
I2C0
I2C1
SPI1
MCASP1
ETH1
MDIO
ETH2
LCD
ADC0
ADC1
GPIOS
TOP LAYER
BOT LAYER
P600
TE_2013022
GREEN = AM437X BALL NUMBER
ORANGE = TPS65218 PINS
Title/Version/Variant: MISDIMMAM437X018_H111
Drawn By: Sebastian Bleicher
Size: A2
Date: 23.10.2015
Time: 10:13:14
Sheet 7 of 8
File: M:\Altium_Designer\Projects\MISDIMMAM437X018_H110\PRJ\SCH\MISDIMMAM437X018_H110_CON.SchDoc
Company Address:
MIS
Lohwiese 7
86937 Scheuring
R. Mannhardt Industrie Systeme
www.mistec.de

5 . Mechanical Specifications



For a better mechanical stability the MIS-DIMM-AM437X can be fasten to the carrier board using the mechanical hole in the upper right corner.

Diameter: 2.5mm for a M2.5 screw

The mounting hole is NOT connected to GND.

6 . RoHS compliance

MIS-DIMM-AM437X System-on-Module complies with the European Union Restriction on Use of Hazardous Substance Directive 2002/95/EC (“RoHS 1”), Directive 2011/65/EU (“RoHS 2”).

7 . Ordering Information

Please refer to www.mibtec.de

8 . Warranty Terms

MIS guarantees hardware products against defects in workmanship and material for a period of one year from the date of shipment. Your sole remedy and MIS sole liability shall be for MIS, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

8.1 Disclaimer of Warranty

This warranty is made in lieu of any other warranty, whether expressed, or implied, of merchantability, fitness for a specific purpose, non-infringement or their equivalents under the laws of any jurisdiction, except the warranty expressly stated herein. The remedies set forth herein shall be the sole and exclusive remedies of any purchaser with respect to any defective product.

8.2 Limitation on Liability

To the maximum extent permitted by law, MIS is not liable under any contract, negligence, strict liability or other legal or equitable theory for any loss of use of the product, inconvenience or damages of any character, whether direct, special, incidental or consequential (including, but not limited to, damages for loss of good will, loss of revenue or profit, work stoppage, computer failure or malfunction, failure of other equipment) resulting from the use of the product, relating to warranty service, or arising out of any breach of this limited warranty, even if MIS has been advised of the possibility of such damages.

MIS products are not authorized for use in safety-critical applications (such as life support) where a failure of the MIS product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of MIS products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by MIS. Further, buyers must fully indemnify MIS and its representatives against any damages arising out of the use of MIS products in such safety-critical applications.

The sole remedy for a breach of the foregoing limited warranty is repair, replacement or refund of the defective or non-conforming product. The maximum liability of MIS under this warranty is limited to the purchase price of the product covered by the warranty. The foregoing express written warranties and remedies are exclusive and are in lieu of any other warranties or remedies, express, implied or statutory.

9 . About MIS

MIS is located in the southern part of Bavaria/Germany. Our core competencies are developing and manufacturing electronics. Today MIS is a full service provider starting from a customers product idea or specification, HW- and SW development, product certifications. Also we have our own production facility, so everything is produced in house. We offer design services from full custom solutions to very specialist area.

Product-ready System on Modules (SOMs) and development kits based on TI processors allow product designers to begin developing quickly. MIS provides its customers with a complete development kit supporting Openembedded/Yocto/Poky Linux and Android.
MIS can also assist at any point in the product development process: from interaction and industrial design to electrical, mechanical, and software engineering to test development and manufacturing.
Our experience in both hardware design and embedded software development allows us to deliver complete solutions to our clients.
The services include but are not limited to, driver development, RTOS/OS porting, board support packages, video streaming applications based on TI AM437x, specific algorithm design in C/C++, board layout. MIS offers development kits and system-on-modules based on TI's AM437x processor to meet customers different requirements.

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